





20. The method of claim 19 wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design.

21. The method of claim 19 wherein the statistical estimates correspond to the weighted average of the statistical data generated.

22. The method of claim 21 wherein the weighted average is based on a predetermined number or percentage of the slowest delays.

23. The method of claim 21 wherein the weighted average is based on a predetermined number or percentage of the fastest delays.

24. A computer program product comprising:  
a machine readable memory on which is provided program instructions for a method of placing a source electronic design into a target hardware device by partitioning methods, the instructions comprising:  
code for receiving an electronic representation of the source electronic design;  
code for determining a path criticality in the source electronic design based on determining an actual delay corresponding to a connection already placed across a first boundary in the target device,  
code for determining a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device; and  
code for partitioning at least a portion of the source design by placing the at least a portion of the source design across boundaries in the target device based on the criticalities determined.

25. The computer program product of claim 24 wherein the code for determining the statistical estimate for future delay comprises:  
code for receiving at least one source design;

code for placing the at least one source design using partitioning methods to place the device across boundaries in the target device; and

code for generating statistical data corresponding to each type of boundary crossed in the target device,

wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design

26. The computer program product of claim 25 wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design.

27. The computer program product of claim 26 wherein the statistical estimates correspond to the weighted average of the statistical data generated.

28. The computer program product of claim 27 wherein the weighted average is based on a predetermined number or percentage of the slowest delays.

29. The computer program product of claim 28 wherein the weighted average is based on a predetermined number or percentage of the fastest delays.

30. A computer system having a central processing unit (CPU) coupled to a memory, comprising:

an interface for communicating with an individual;

wherein the computer system is configured to receive an electronic representation of the source electronic design;

wherein the computer system is further configured to,

determine a path criticality in the source electronic design based on determining an actual delay corresponding to a connection already placed across a first boundary in the target device, and

determine a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device; and

wherein the computer system is further configured to partition at least a portion of the source design by placing the at least a portion of the source design across boundaries in the target device based on the determined actual delay.

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